

ELC 4438: Embedded System Design

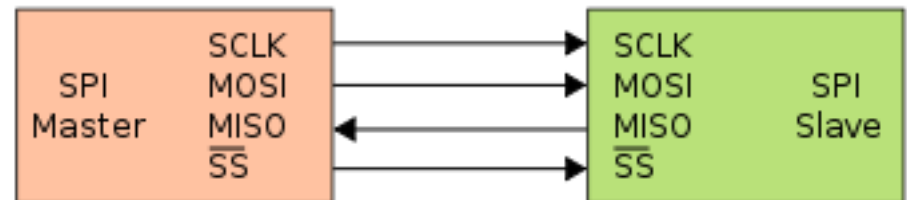
Serial Peripheral Interface Bus

Liang Dong

Electrical and Computer Engineering
Baylor University

Serial Peripheral Interface Bus

- SPI bus is a synchronous serial communication interface for short distance communication.
- SPI devices communicate in full duplex mode using a master-slave architecture with a single master.
- Multiple slave devices are supported through selection with individual slave select (SS) lines.
- SPI a *four-wire* serial bus.

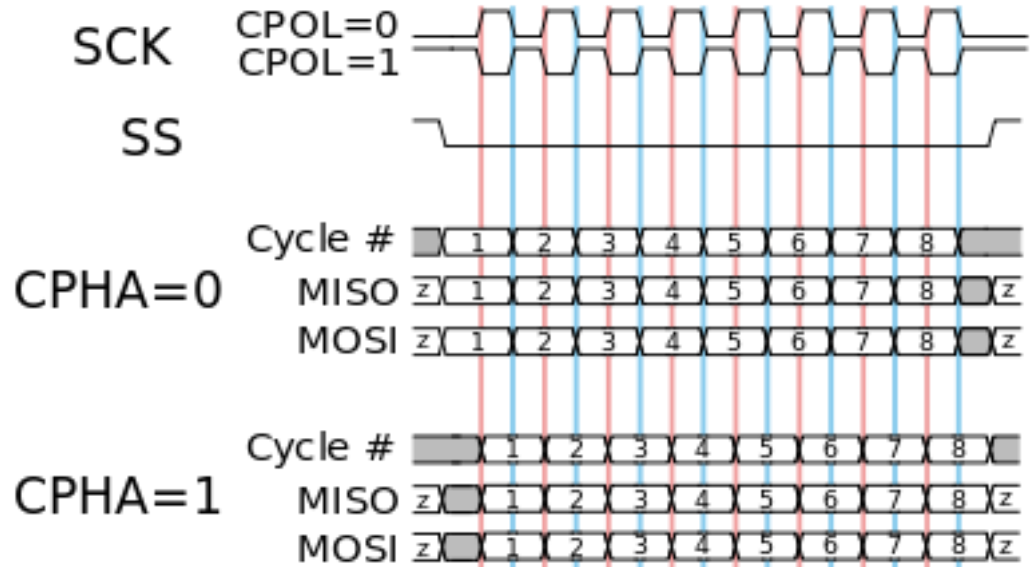
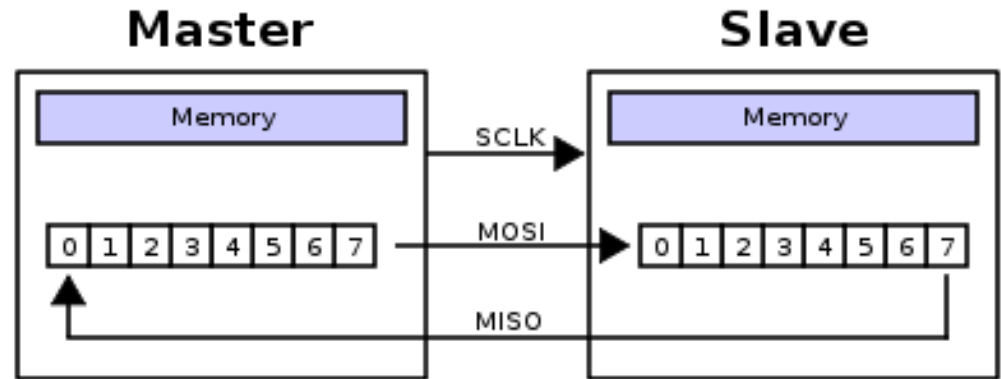


Data Transmission

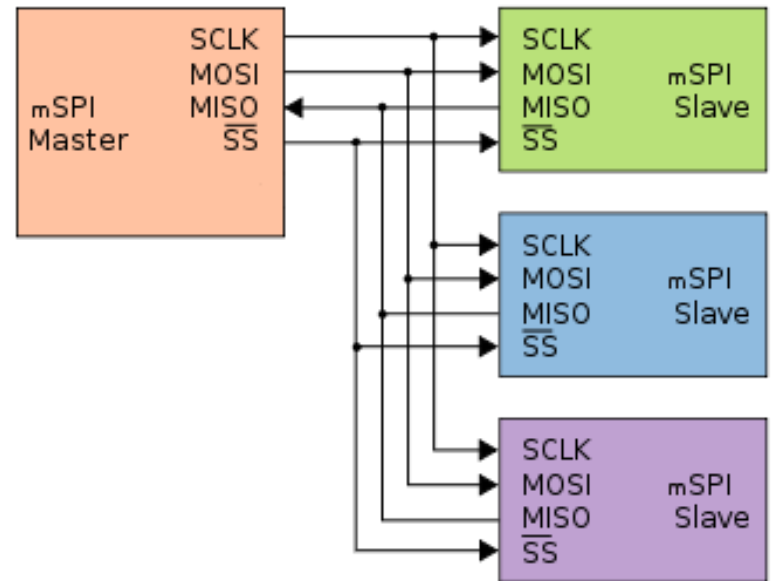
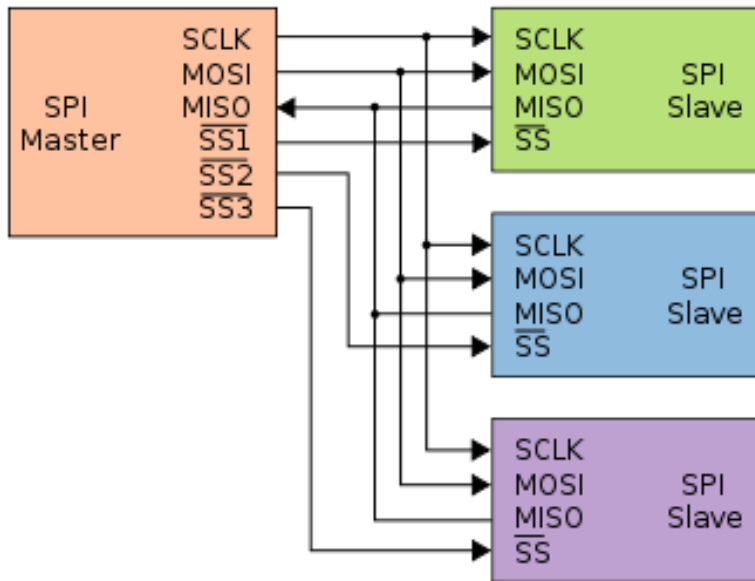
- The bus master configures the clock, using a frequency supported by the slave device, typically up to a few MHz.
- The master then selects the slave device with a logic level 0 on the select line. The master must select only one slave at a time.
- During each SPI clock cycle, a full duplex data transmission occurs. Two shift registers

Data Transmission

- Two shift registers

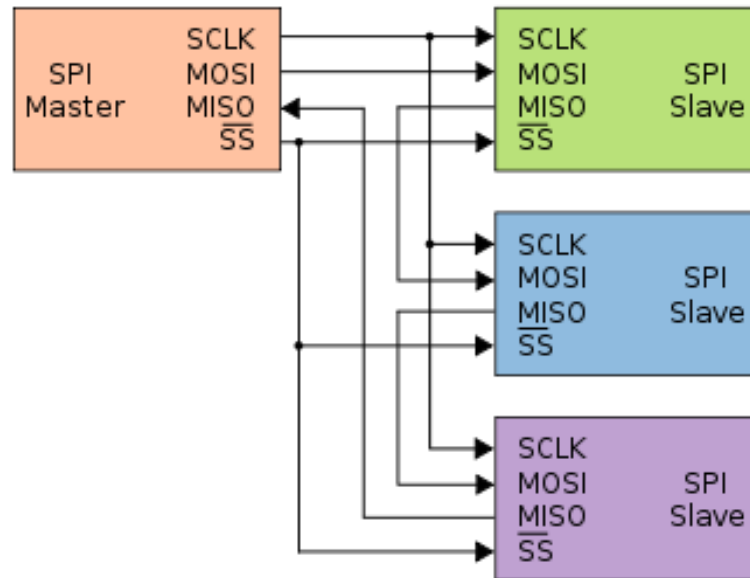


SPI Bus Structure



With "slave address"

SPI Bus Structure



Daisy-chained SPI bus: master and cooperative slaves